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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,516	FLOMAN ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/828,516 has a total of 23 claims pending in the application; there are 2 independent claims and 21 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submission of the Information Disclosure Statement dated August 1, 2005 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. OBJECTIONS TO THE SPECIFICATION

Claim Objections

5. Claims 16-17 are objected to because of the following informalities:

Claim 11 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 11 appears to duplicate the contents of claim 10; the claim on which it depends.

As per **claim 16**, the word "provide" (line 2) appears to be a typographical error. It is believed this word should be – **provides** – and has been treated as such for the rest of this office action.

As per **claim 17**, the word "to" (line 3) appears to be a typographical error. It is believed this word should be – **through** – and has been treated as such for the rest of this office action.

6. Appropriate correction is required.

Specification Objections

7. The disclosure is objected to because of the following informalities:

The word "area" (page 1, line 8) appears to be a typographical error. It is believed this word should be –**areas**- and has been treated as such for the rest of this office action.

The word "signal" (page 4, line 18) appears to be an error. It is believed this word should be –**single**- and has been treated as such for the rest of this office action.

8. Applicant's cooperation is requested in correcting any other errors of which applicant may become aware in the specification.

9. Appropriate correction is required.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. **Claims 1-8, 12-14, 18-19, and 21-23** are rejected under 35 U.S.C. 102(b) as being anticipated by Six et al. (US 6,898,678).

12. As per **claims 1 and 21-22**, Six discloses

"A memory unit with at least two memory areas for storing data," as **["memory 42" which has memory areas "42a" and "42b" (Figures 1 and 2). Six also discloses Fig. 4 which has SARAM 220, DARAM 222 and ROM 224]**

"first terminals for accessing data within the memory areas, and second terminals for accessing data within the memory areas," **[With respect to this limitation, Six discloses "bus 11" and "bus 21" and access ports to "memory 42" shown by arrows (Figures 1 and 2)]**

"a first processor in communication with a memory unit" **[Six discloses this limitation as "host processor 10" (Figures 1 and 2)]**

"second processor in communication with the memory unit" **[Six discloses this limitation as "DSP processor 20" (Figures 1 and 2)]**

"characterised by at least two access control means for providing selectively sole addressing and accessing data through one of the terminals," by one of the processors **[With respect to this limitation, Six discloses "HOM (Host Only Memory)" access mode wherein "host only memory 42a is accessed directly in HOM mode by bus 11 in a manner that bypasses scheduler 40" (Column 3, lines 39-42 and Figures 1 and 2) and explains that in "host only mode (HOM), only the MCU can access the SARAM" (Column 10, lines 44-45)]** "or individual addressing and accessing data through each of the terminals, respectively" by each of the processors, respectively **[Six discloses this limitation as "SAM (Shared Access Memory)" mode, in which access to the memory circuit is shared between the plurality of requestor circuits (Column 2, lines 27-29) and explains that "in shared access mode (SAM) both the MCU and DSP may access the SARAM" (Column 10, lines 40-42) and the "DARAM" (Columns 9-10, lines 58-67 and 1-46)]**.

13. As per **claim 2**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein the first and/or second terminal comprises control ports for receiving control signals for controlling access to the memory areas" **[Six discloses this limitation as "a DMA (direct memory access controller)" which is connected to each of the memory resources wherein "each port has an associated port control block 360-363. These blocks are responsible for initiating the read/write accesses to the memories and peripherals" (Column 7, lines 39-41 and Figure 6)]**.

14. As per **claim 3**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein the first and/or second terminal comprises address ports for receiving addressing signals for addressing data within the memory areas" **[With respect to this**

limitation, Six discloses "a DMA (direct memory access controller)" in which "a read address bus RA includes seven individual buses for conveying a channel read address form each read address unit RAU (0-5) and from the HPI port to each port input mux 330-333 in parallel" (Column 6, lines 62-65 and Figure 6)].

15. As per **claim 4**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein the first and/or second terminal comprises data ports for reading and/or writing data to and/or from the memory areas" **[Six discloses this limitation as a "DMA (direct memory access) controller" wherein "a port can make read and write accesses to the resource to which it is connected, through a dedicated bus" (Column 6, lines 28-30 and Figure 6)].**

16. As per **claim 5**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein the access control means provide access to the data areas based on control and/or address signals at said terminals" **[Six discloses this concept as "each memory bank 50(n) has a multiplexor 52 that receives bus 11 on one input and bus 41 on a second input. Mux control circuit 53 provides a control signal to select bus 11 when the HOM bit is asserted and a respective HOM size enable signal is asserted. Otherwise, mux 52 selects bus 41. An output node of each mux provides the selected request signal, including address and data, to the associated memory bank" (Column 4, lines 23-30)].**

17. As per **claim 6**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein the access control means are state machines, the state machines providing access to the data areas based on states of signals at the first and second terminals" **[Six discloses**

this limitation as transitions from one access mode to another is controlled by state machine 662 (Column 9, lines 38-67, Column 10, lines 1-46 and Figures 7A and 7B)].

18. As per **claim 7**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein the access control means comprise memory registers" **[With respect to this limitation, Six discloses a "priority circuitry" which "is implemented in the SARAM, whereas the control register is located in the DMA 10 space accessible via RHEA bus branch 130a" (Column 5, lines 20-23) wherein "control register" is defined as "A DMA Enable/Disable Control Register (DMEDC)" (Figure 6)].**

19. As per **claim 8**, Six discloses "The memory unit of claim 3," **[See rejection to claim 3 above]** "wherein the address ports provide access to an external address bus" **[With respect to this limitation, Six discloses "EMIF (External Memory Interface)" which provides access and control to "External memory 122" (Figure 3)].**

20. As per **claim 12**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein at least two memory areas are provided" **[Six discloses this limitation as "memory 42" which has memory areas "42a" and "42b" (Figures 1 and 2). Six also discloses Fig. 4 which has SARAM 220, DARAM 222 and ROM 224].**

21. As per **claim 13**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein programming the size of the memory areas is provided through one of the terminals" **[With respect to this limitation, Six discloses that "memory block 42 has a total size S1. Host only memory 42a has a size S2 that is selected for a particular application, for example. Shared memory portion 42b has a size S3 that is equal to S1 minus S2" and**

explains that "size S1 can be changed under control of host processor 110" (Column 3, lines 44-51 and Figure 1)].

22. As per **claim 14**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein three memory areas are provided" **[Six discloses this limitation as "memory 42" which has memory areas "42a" and "42b" (Figures 1 and 2) each comprising different memory banks. Six also discloses Fig. 4 which has SARAM 220, DARAM 222 and ROM 224].**

23. As per **claim 18**, Six discloses "The memory unit of claim 1," **[See rejection to claim 1 above]** "wherein one of the terminals provides accessing the data by a central processing unit, and wherein one of the terminals provides accessing the data by a graphics processor" **[With respect to this limitation, Six discloses "host processor 10" and "DSP 20" which is defined as a digital signal processor (Figure 1 and Column 3, lines 23-43)].**

24. As per **claim 19**, Six discloses "The method unit of claim 1," **[See rejection to claim 1 above]** "wherein the bandwidth and/or clocking frequency for the terminals is different" **[Six discloses this concept as in HOM (host only memory) mode, "a portion of the memory is connected directly to one of the requesters, such as a host processor, so that high bandwidth transfers can be performed" while, at the same time, "a portion that is not selected in HOM can be accesses by other requestors" (Column 12, lines 1-11) in "a low power state without affecting transfers by the host processor" (Column 8, lines 17-30)].**

25. As per **claim 23**, Six discloses the invention as specified in claim 1 **[See rejection to claim 1 above]** "A mobile communication device comprising a memory unit of claim 1" **[With respect to this limitation, Six discloses an example of an integrated circuit according to the**

invention in a mobile telecommunications device, such as a mobile telephone (Column 11, lines 31-39 and Figure 11)].

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. **Claims 9-11, 15-17 and 20** rejected under 35 U.S.C. 103(a) as being unpatentable over Six et al. (US 6,898,678) in view of Roy (US 6,065,092).

28. As per **claims 9-11, 15-16 and 20**, Six discloses "A method for providing access to a memory unit of claim 1 by receiving access signals and providing data from memory areas through first terminals, and receiving access signals and providing data from memory areas through second terminals" **[See rejection to claim 1 above]** but does not disclose expressly "receiving access signals solely through one terminal and providing data from memory areas through both terminals, or receiving access signals and providing data from memory areas through both terminals individually, respectively."

Roy discloses the concept of "receiving access signals solely through one terminal and providing data from memory areas through both terminals, or receiving access signals and providing data from memory areas through both terminals individually, respectively" as **[a multichannel memory architecture which "permits a plurality of master devices to be**

coupled to the multi-line channels for conducting selected data read and/or write transactions within the clusters;" providing "a plurality of distinct operating modes for the selected data read and/or write transactions" (Column 7, lines 31-37) wherein in an "independent mode," "independent data read and/or write transactions can occur simultaneously within distinct ones of the clusters through distinct ones of the multi-line channels" "" in a "cooperative mode," "a first one of the multi-line channels provides address and control information for a particular transaction and a second one of the multi-line channels provides data associated with the particular transaction" and in "a synchronous mode," "at least two of the multi-line channels are synchronized together to provide a wider effective channel to provide data associated with a particular read and/or write transaction to two or more clusters simultaneously" (Column 7, lines 45-49) and explains that "at any given moment, the data channels can operate either independently of each other within different regions of the memory device, or can cooperate intelligently with each other to operate more efficiently within one particular region of the memory device. These modes of operation may be constantly changing during normal operation of the memory device" (Column 9, lines 31-37)].

Six et al. (US 6,898,678) in view of Roy (US 6,065,092) are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory unit which provides an access mode in which a single unit accesses a memory system or multiple unit access a memory system as taught by Six and further

selectively provide data related to an input/output transaction through single or multiple channels/ports as taught by Roy.

The motivation for doing so would have been because Roy teaches that selectively providing data for input/output transactions through single or multiple channels/ports by "receiving access signals solely through one terminal and providing data from memory areas through both terminals, or receiving access signals and providing data from memory areas through both terminals individually" **[provides a highly flexible architecture as "it permits multiple separate data channels to operate either independently from each other, cooperatively (in which one channel provides address and control information for a data transfer on another channel), or synchronously (in which multiple channels are operated concurrently to provide a wider effective channel for a particular data transfer operation)" (Column 9, lines 4-10) and also provides faster and more efficient utilization of a memory device as the system can selectively adapt to different data width requirements by increasing "the effective width of the total data bus to larger values for a particular data read or write transaction" by having "subsequent transfer of data on each of these channels" synchronized to "provide an effectively wider channel" (Column 10, lines 23-32)]**.

Therefore, it would have been obvious to combine Roy (US 6,065,092) with Six et al. (US 6,898,678) for the benefit of creating a memory unit to obtain the invention as specified in claims 9-11, 15-16, and 20.

29. As per **claim 17**, the combination of Six and Roy discloses "The memory unit of claim 16," **[See rejection to claim 16 above]** "wherein the access control means provide prioritised

access to the third memory area to one of the terminals" **[Six discloses this concept as "in host only mode, a portion of the memory is connected directly to one of the requesters, such as host processor, so that high bandwidth transfers can be performed. A portion that is not selected to be in HOM can be accessed by other requestors or shut down to save power" (Column 12, lines 1-11) and explains that "in HOM mode, the HPI module has exclusive access to the SARAM" (Column 11, lines 9-11 and Column 8, lines 17-30). Also note figures 7A and 7B which explain transitioning from SAM mode to HOM mode and from HOM mode to SAM mode, respectively]**.

VI. RELEVANT ART CITED BY THE EXAMINER

30. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

31. The following reference teaches a multi-port memory having single or dual access modes.

U.S. PATENT NUMBER

US 4,893,279

32. The following reference teaches a dual port memory partitioned so that each portion is used by a different processor.

U.S. PATENT NUMBER

US 5,329,630

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

33. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

34. Per the instant office action, claims 1-23 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

36. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 4, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER